# MAXIM Engineering Journal

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# News Briefs

## MAXIM REPORTS RECORD REVENUES AND EARNINGS FOR THE FIRST QUARTER OF FISCAL 2000

Maxim Integrated Products, Inc., (MXIM) reported record net revenues of $180.0 million for the first quarter of fiscal 2000 ending September 25, 1999, compared to $155.3 million for the same quarter in fiscal 1999. Net income increased to a record $58.4 million in Q100, compared to $49.4 million for the first quarter of fiscal 1999. Diluted earnings per share were $0.37 for Q100, compared to $0.33 for the same period a year ago.

During the quarter, the Company increased cash and short-term investments by $64.6 million after paying $36.2 million for 525,000 shares of its common stock and $26.8 million for capital equipment. Accounts receivable increased in Q100 to $93.1 million due to the increase in net revenues, while inventories declined slightly to $44.9 million during the quarter.

Gross margin for the first quarter was consistent with Q499 at 69.7%. During the quarter, the Company recorded a writedown of equipment of $2.5 million and increased inventory reserves by $1.8 million. The Company also recorded a charge to selling, general, and administrative expenses of $1.5 million related to technology licensing matters.

Bookings on the Company were approximately $242 million in Q100, a 22% increase over the Q499 level of $198 million. During the quarter, customers continued their trend of ordering for near-term delivery. Turns orders received in Q100 were $101 million, compared to the Q499 level of $81 million (turns orders are customer orders that are for delivery within the same quarter and may result in revenue within the same quarter if the Company has available inventory that matches those orders).

End-market bookings increased 23% over Q499 levels (end-market bookings are end-user customer bookings received by both Maxim and the Company's distributors during the quarter). This increase was fueled by double-digit end-market bookings growth in the U.S., Pacific Rim, Japan, and Europe. Bookings increased across all major product lines during the quarter.

First quarter ending backlog shippable within the next 12 months was approximately $225 million, including $192 million requested for shipment in the second quarter of fiscal 2000. Last quarter, the Company reported fourth quarter ending backlog shippable within the next 12 months of approximately $176 million, including $144 million that was requested for shipment in Q100. Order cancellations remained low during Q100 at approximately $11 million, compared to $13 million in Q499.

Jack Gifford, Chairman, President, and Chief Executive Officer, commented on the quarter: "Q100 was an excellent quarter, with record revenues and earnings. Bookings growth once again exceeded our expectations. We were encouraged to see increased bookings in all geographical regions and across a broad spectrum of end markets. Our backlog, which was significantly depleted during fiscal 1999, is now at a healthy level. We expect that in future quarters, our bookings growth rate will moderate to levels reflective of our forecasted demand for Maxim products in fiscal 2000."

Mr. Gifford continued: "During the quarter, we continued to invest in our future, with research and development spending of $28.3 million during Q100, an 18% increase over Q499 spending of $24.0 million and a 34% increase over one year ago. This spending is in line with our continuing commitment to define, develop, and introduce new products and to develop innovative new processes during fiscal 2000.

"The communications and portable equipment markets have long-term growth opportunities that we believe will significantly increase the size of the mixed-signal analog market of the next 5 years. Maxim appears to have accomplished a successful entry into these areas, allowing for future growth."

# SiGe technology enhances radio front-end performance

*Three parameters are increasingly important for cellular handsets and other digital, portable, wireless communication devices. Low power consumption and lightweight batteries lend autonomy to the device, higher front-end sensitivity increases the reception distance, and greater front-end linearity has a direct impact on the admissible dynamic range. This last parameter is gaining emphasis with the advent of nonconstant-energy modulation schemes such as π/4DQPSK and 8QAM.*

GST-3 is the newest innovation for simultaneously improving the power consumption, sensitivity, and dynamic range of a receiver. GST-3 is a new high-speed IC process technology based on silicon germanium (SiGe), which features a transition figure ($f_T$) of 35GHz. A typical front-end block diagram (**Figure 1**) shows the performance possible with SiGe technology (1.9GHz) for a combination mixer and low-noise amplifier (LNA).

## Noise performance

The main contribution to noise figure in the down-conversion link is noise created by the LNA's first transistor input stage. Noise figure (NF) serves as a figure of merit for networks, to compare noise in the actual network with that in an ideal noiseless network. The noise factor (F) for an amplifier or other network with power gain (G) equal to $G = P_{OUT}/P_{IN}$ can be expressed as:

$$F = \frac{\text{(amplifier's actual, measured output noise power)}}{\text{(amplifier's output noise power due to } R_{SOURCE}\text{)}}$$

NF is a measure of the degradation in the signal-to-noise ratio (SNR) between the input and output ports of a network, typically expressed in dB: $NF = 10\log_{10}F$. Therefore,

$$\begin{aligned} F &= \text{Input SNR/Output SNR} \\ &= (P_{IN}/N_{IN})/(P_{OUT}/N_{OUT}) \\ &= N_{OUT}/(N_{IN} \cdot G) \end{aligned}$$

We are concerned with thermal noise (also called Johnson noise or white noise) and shot noise (also called Schottky noise). A detailed high-frequency equivalent model for the bipolar transistor (the Giacoleto model—see **Figure 2**) helps in understanding how this noise is generated. The model also shows how SiGe technology can help reduce the LNA's front-end noise figure.

## Thermal and shot noise

Within a conducting medium whose temperature is above absolute zero (0°K), the random motion of charge carriers produces random noise-producing voltages and currents. A rising conductor temperature increases the charge-carrier velocity of these random motions, which

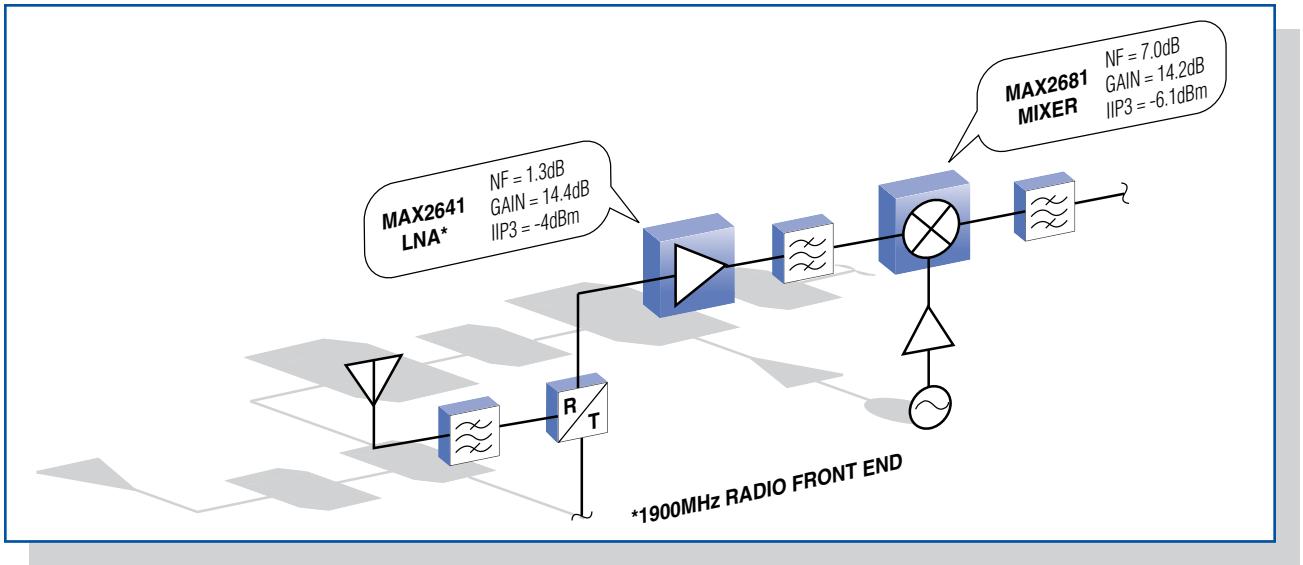


*Figure 1. Typical radio input circuitry includes a low-noise amplifier and mixer.*

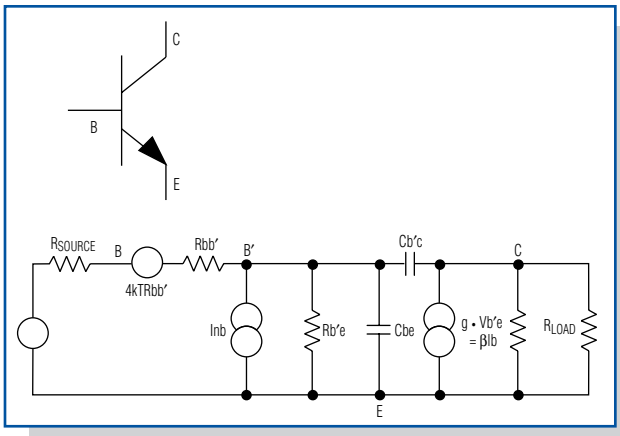


*Figure 2. This detailed NPN-transistor model (the Giacoleto model) simplifies the analysis of frequency effects.*

increases the noise voltage. The thermal noise generated by parasitic base resistance (Rbb′) in a transistor is Vn(f) = 4kTRbb′, where Vn(f) equals the voltage spectral noise density in $V^2/Hz$. The k is Boltzmann's constant ($1.38 \cdot 10^{-23}$ Joules/Kelvin), and T is the absolute temperature in degrees Kelvin (°C + 273°).

Shot noise is a consequence of the particle-like nature of charge carriers. DC current flow in a semiconductor is often regarded as constant at every instant, but any current consists of individual electrons and holes. Only the time-average flow of these charge carriers appears as constant current. Any fluctuation in the number of charge carriers produces a random current at that instant, which is known as shot noise.

The spectral noise density for shot noise in the base current is Inb(f) = 2qIb = 2qIc/β, where Inb is the current spectral noise density in $I^2/Hz$, Ib is the base DC-biasing current, q is one electron charge ($1.6 \cdot 10^{-19}$ coulombs), and β is the transistor's DC current gain. Thus, the total noise spectral density generated by the transistor's input stage is the sum of the thermal and shot noise:

$$\gamma n = 4kTRbb' + R_{SOURCE}\, 2qIc/\beta$$

Maxim's new SiGe process, GST-3, was created as an extension of GST-2 (a bipolar process with a transition frequency of 27GHz) by doping the transistor bases with germanium. The result was an important decrease in Rbb′ and a significant increase in the transistor beta. The combined effect of these two changes is better noise figure for the SiGe transistor (vs. that of a silicon transistor with similar collector current). Typically, the transistor noise figure is expressed as:

$$F = 1 + \frac{\left[Vn^2(f)/R_{SOURCE} + Inb^2(f) \cdot R_{SOURCE}\right]}{4kT}$$

Because $R_{SOURCE}$ = Vn(f)/Inb(f) gives a minimum noise figure for Si-bipolar as well as SiGe technology, the full benefits of the SiGe process can be obtained by designing an LNA with source impedance close to this value.

Another important aspect of wireless design is the derating of noise figure vs. frequency. The power gain of a typical transistor is similar to the upper curve in **Figure 3**. This curve is not surprising, considering the equivalent transistor circuit of Figure 2. In effect, the model is an RC lowpass filter whose gain falls off at 6dB per octave. The maximum theoretical frequency for which the common-emitter current gain (β) is unity (0dB) is called the transition frequency ($f_T$). An LNA's gain (G) depends directly on β, so the derating of noise figure [$F = N_{OUT}/(N_{IN}G)$] begins with the rolloff of gain.

To see how the GST-3 SiGe process improves noise figure at high frequencies, consider that adding germanium to the P-silicon base of a transistor reduces the bandgap by 80mV to 100mV across the base, creating a strong electric field between the emitter and collector junctions. By rapidly sweeping electrons from the base into the collector, this electric field reduces the transit time ($t_b$) required for carriers to cross the narrow base. If all other factors are held constant, this reduced $t_b$ provides an approximate 30% increase in $f_T$.

For identical-area transistors, the GST3 device achieves a given $f_T$ with one-half to one-third the current required in a GST-2 device. Higher $f_T$ reduces high-frequency noise, because the β rolloff occurs at a higher frequency.

## Ultra-low-noise SiGe amplifier (MAX2641)

The MAX2641 offers advantages over silicon-bipolar LNAs, whose NF falls off for frequencies approaching the 2GHz limit (i.e., 1.5dB at 1GHz vs. 2.5dB at 2GHz). High reverse isolation in the SiGe device also allows

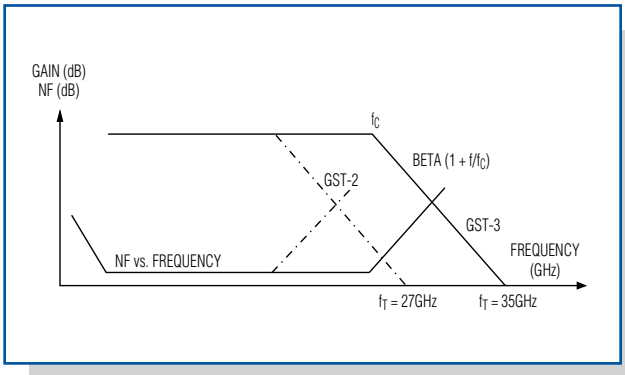


*Figure 3. SiGe bipolar transistors exhibit high gain and low noise.*

tuning of the input-matching network without affecting the output matching, and vice versa.

The MAX2641 is optimized for operation in the 1400MHz to 2500MHz range, with typical performance that includes 14.4dB gain, -4dBm input IP3 (IIP3), 30dB reverse isolation, and a 1.3dB noise figure at 1900MHz **(Figure 4)**. Available in 6-pin SOT23 packages, it operates from a +2.7V to +5.5V single supply, draws 3.5mA, and is internally biased. The only external components typically required are a two-element input match, input and output blocking capacitors, and a $V_{CC}$ bypass capacitor.

## Linearity

In addition to noise and finite bandwidth, communication systems are limited by signal distortion. The system's usefulness depends on its dynamic range (i.e., the signal range it can process with high quality). Dynamic range is dictated by noise figure, whose lower limit is defined by the sensitivity level and whose upper limit is defined by the acceptable maximum level of signal distortion. Achieving the optimum dynamic range involves trade-offs among power consumption, output signal distortion, and the level of input signal with respect to noise.

A typical receiver block diagram (Figure 1) shows the relative importance of noise figure and linearity for the LNA and mixer. Because the LNA input is supplied directly by a very low-level signal from the antenna, its NF is the dominant parameter. For the mixer, fed by an amplified signal from the LNA output, linearity is the dominant parameter.

The output is never an exact replica of the input signal because no transistor is perfectly linear. The output signal always includes harmonics, intermodulation distortion (IMD), and other spurious components. In **Figure 5**, the second term of the $P_{OUT}$ equation is called the second harmonic or second-order distortion, and the third term is called the third harmonic or third-order

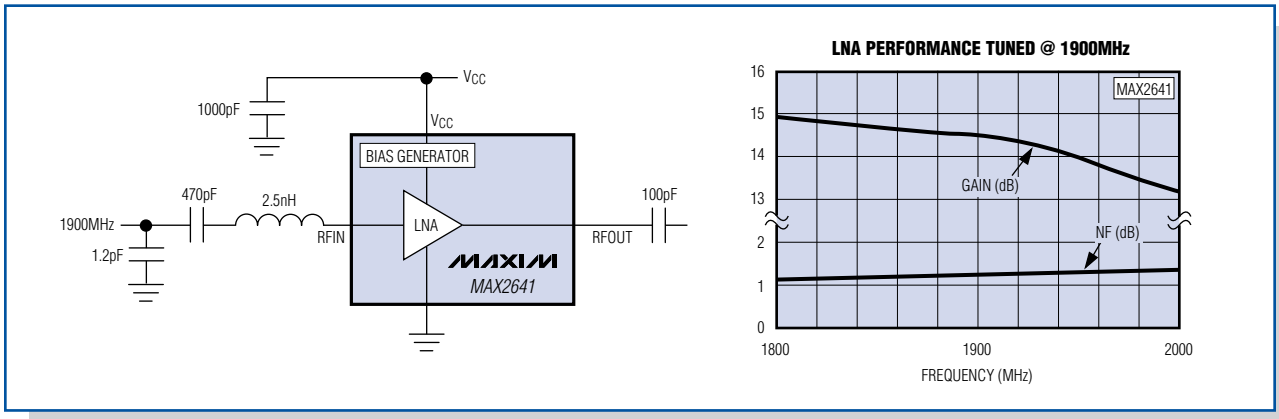


*Figure 4. Note the very low noise figure for this integrated-circuit low-noise amplifier.*

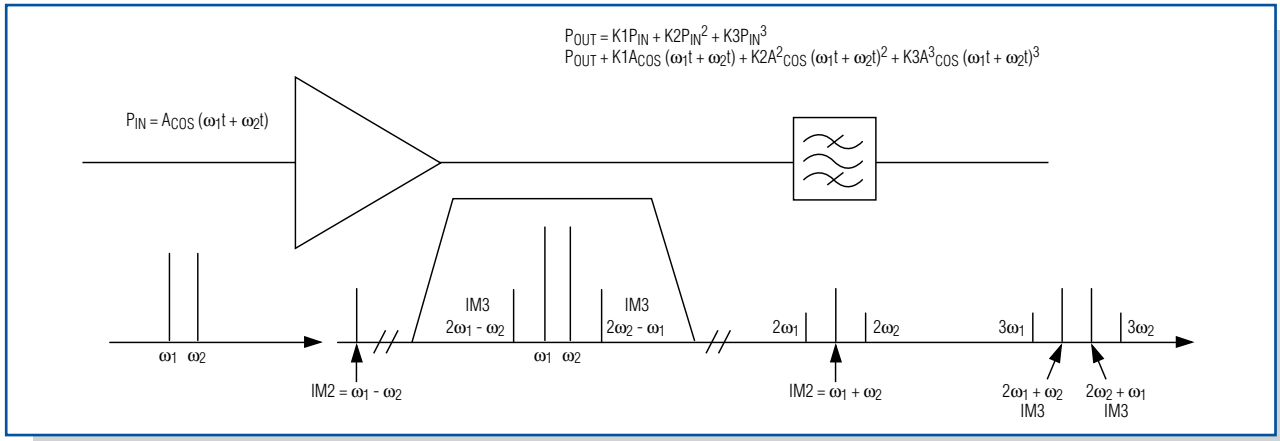


*Figure 5. A two-tone test characterizes harmonic and intermodulation distortion.*

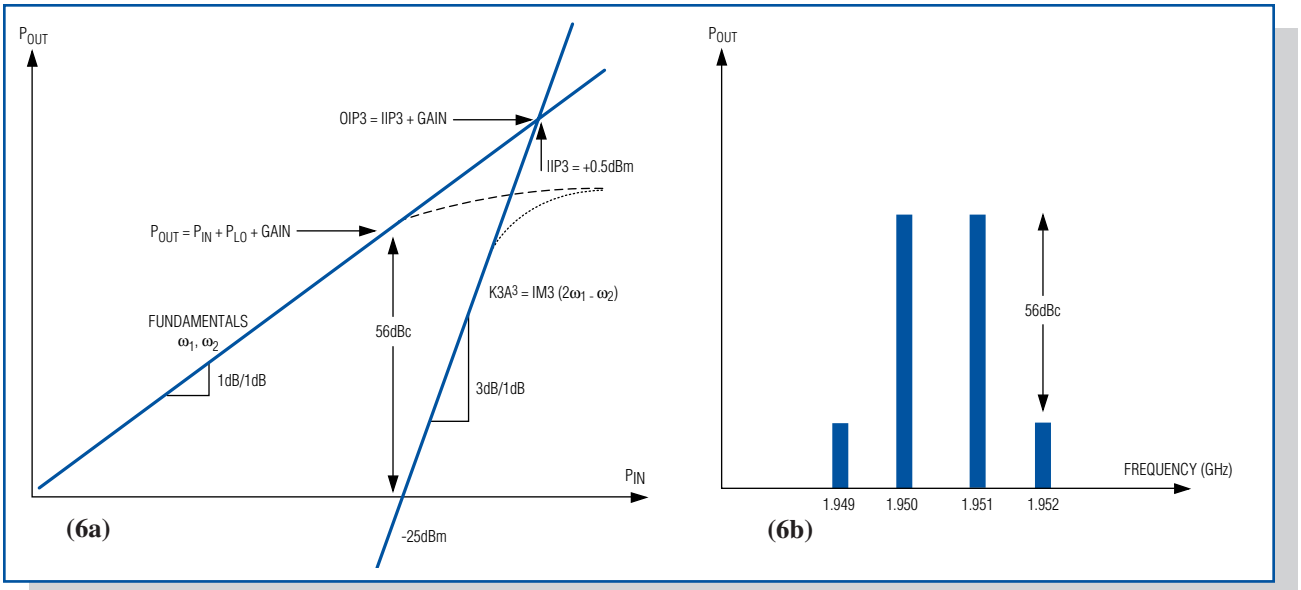


*Figure 6. This SiGe double-balanced downconverter provides a low (0.5dBm) IIP3 level* ***(a)*** *and a 56dBc dynamic range* ***(b)****.*

distortion. Both are characterized by driving the device input with a signal consisting of one tone or two pure sinusoidal tones closely spaced in frequency. Third-order intermodulation distortion for the MAX2681, for example, is characterized with a -25dBm signal consisting of tones at 1950MHz and 1951MHz.

A graphic frequency-domain representation of the $P_{OUT}$ equation shows that the output consists of fundamental frequencies $\omega_1$ and $\omega_2$, second harmonics $2\omega_1$ and $2\omega_2$, third harmonics $3\omega_1$ and $3\omega_2$, the second-order intermodulation product IM2, and the third-order intermodulation product IM3. Figure 5 also shows that in cellular handsets and other systems with narrow-band operating frequencies (i.e., a few tens of megahertz, and less than an octave), only the IM3 spurious signals $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ fall within the filter passband. The result can be distortion in the desired signals associated with $\omega_1$ and $\omega_2$.

In the $P_{OUT}$ equation for low levels of output power, coefficient K1A is directly proportional to the input signal amplitude, $K2A^2$ is proportional to the square, and $K3A^3$ is proportional to the cube of the input amplitude. Thus, the plot of each on a log scale is a straight line with slope corresponding to the order of the response.

Second- and third-order intercept points are often used as figures of merit. The higher the intercept point, the better the device can amplify large signals. At higher power levels, the output response is compressed and therefore deviates from the response of the fundamental. This deviation point **(Figure 6a)** is defined as the 1dB compression point, and is situated where the output signal compresses by 1dB ($G_{1dB}$ = G - 1dB) with respect to an extrapolation of the linear portion of the curve.

From the MAX2681 data sheet, $P_{OUT}$ vs. frequency above 1900MHz shows a -56dBc spurious-free dynamic range (SFDR) relative to IM3 **(Figure 6b)**. The typical operating conditions are $P_{RFIN}$ = -25dBm, IIP3 = 0.5dBm, and conversion gain = 8.4dB. LO-to-IF leakage and other spurious artifacts can be filtered by a narrow-bandpass IF filter, as shown in Figure 1. The MAX2681 (a SiGe double-balanced downconverter) achieves this performance with typical $I_{CC}$ currents of only 8.7mA.

Another downconverter mixer (MAX2680) offers different performance specifications. Available in a miniature 6-pin SOT23 package, it consists of a double-balanced Gilbert-cell mixer with single-ended RF, LO, and IF port connections. Like the MAX2681, it operates from a single +2.7V to +5.5V supply, accepts RF inputs between 400MHz and 2500MHz, and downconverts to IF outputs between 10MHz and 500MHz. Supply current in shutdown mode is typically less than 0.1µA. The LO input is a single-ended broadband port whose typical input VSWR (400MHz to 2.5GHz) is better than 2.0:1.

## Front-end input sensitivity

To evaluate the front-end sensitivity achievable using MAX2641/MAX2681 downconverters, consider QPSK modulation with a 4MHz signal bandwidth. To simplify calculations, assume a perfect rectangular input filter. First, a 3dB NF (AntNF) must be added to counteract a 3dB insertion loss caused by the antenna switch and

front-end passive filter. Next, a post-LNA filter is added to eliminate distortion (other than IM3 distortion) generated by the LNA. Consider using a filter with 2dB of attenuation and NF for this purpose. At 1900MHz, the post-LNA filter NF adds to the MAX2681's 11.1dB NF:

Total NF = filter NF + mixer NF =
2dB + 11.1dB = 13.1dB

The LNA input needs high NF because it is supplied directly by a very low-level signal from the antenna. The mixer NF is attenuated by LNA gain:

Total NF = LNA NF + $(1/G_{LNA})(NF_{TOTAL} - 1) = 2.054$;
$NF_{TOTAL}$ (dB) = 10log2.126 = 3.12dB.

With QPSK modulation and a $10^{-3}$ BER, the minimum required ratio of bit energy to noise energy at the antenna input is Eb/No = 6.5dB. The absolute noise floor at +25°C is AbsNfl = -174dBm = 10log(KT), where T = +300°K and K = $1.38 \cdot 10^{-23}$. The filter bandwidth in dB is FiltBwth = 10log(4MHz) = 66dB. In Figure 1, the front-end sensitivity for QPSK modulation with $10^{-3}$ BER is estimated as:

Input sensitivity = AbsNfl + AntNF +
FiltBwth + $NF_{TOTAL}$ + Eb/No = -174dBm + 3dB +
66dB + 3.12dB + 6.5dB = -95.38dBm.

## Conclusion

When compared with pure bipolar processes, SiGe provides a lower noise figure vs. frequency for frequencies exceeding 1.0GHz. It also provides lower supply current and higher linearity. Maxim has demonstrated a high-linearity mixer that exhibits a typical IIP3 of 0.5dBm at 1900MHz and a noise figure of 11.1dB (SSB) with conversion gain of 8.4dB, while drawing only 8.7mA of supply current. The higher frequency operation permitted by SiGe's higher transition frequency ($f_T$) enables applications through 5GHz.

## References


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2. Chris Bowick, RF Circuit Designs. (Howard W. Sams, & Co. Inc).
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# Powering portable CPU cores

*Providing electrical power for CPUs and other high-density logic has never been easy, though it appeared for awhile that technology would eventually reduce the power needed for computing tasks. Although technology advances have been rapid, the ever-increasing demand for computing power seems to absorb all improvements and call for more. This appetite for power is especially apparent in notebook computers, whose battery-life extensions have been incremental at best, despite enormous growth in the computing power available per watt.*

Whether this performance plateau results from a need to keep pace with technology or vice versa, the need for higher supply current in portable systems is forcing designers to become familiar with new power-supply technologies. This article explores some of these new technologies.

Shrinking geometries have consistently driven down the supply voltages for CPUs, DSPs, and other large-scale logic devices. Currently in the +1.5V to +2.5V range, these voltages should soon reach 1V. Efficient generation of voltages this low can be a problem, especially for output currents of 10A and up.

As for most electronic designs, an effective power supply must reconcile numerous conflicting goals including cost and component count, efficiency and thermal behavior, circuit size, and transient performance (response to load steps, etc.). Battery life is an issue for portable (battery-powered) systems only, but waste heat (and therefore efficiency) is a major concern for both battery- and AC-powered systems.

## Tighter load regulation + faster response = a losing battle

Today's CPU cores require very tight load regulation. Until recently, the major CPU makers demanded exactly that. But the supply current and clock frequency rise as supply voltages fall, and that places acute demands on the power supply—especially with regard to load-step behavior. The growing difficulty and cost of meeting these ever-tighter performance limits has motivated a rethinking of power-supply design. As just one consequence of higher load currents and larger load transients, the capacitor "farms" that sprout up around a processor add size and cost to a design.

These issues, and the fact that even the fastest switch-mode regulators cannot handle the instantaneous output drop caused by a sudden load step, have forced a change of thinking (and specifications). Output capacitors must do all the work in coping with a step response at the speed of today's CPUs. Furthermore, the tighter load-regulation specs that result in higher open-loop gain require more output capacitance to maintain stability. Thus, it became clear that some way of relaxing the demands of load regulation would pay off generously in reduced component count and in other ways as well.

The response of a typical DC-DC converter to a load step **(Figure 1)** has five basic elements:

1) An instantaneous drop, whose magnitude equals the increase in the load-current step multiplied by the output capacitors' equivalent series resistance (ESR).
2) After the instantaneous drop, there may be a droop before the DC-DC converter responds, in which capacitor voltage falls as the capacitor supplies load current.
3) A voltage-recovery interval, as the inductor switches on to source load current and replenish the output capacitance.
4) An "ESR step-up" as the load is removed (reversing the effect of the instantaneous drop).
5) Some overshoot, as energy stored in the first inductor pulse (after the load falls) is transferred to the output capacitance.

Elements 2, 3, and 5 can be minimized with careful design and a judicious selection of the DC-DC controller. But the instantaneous voltage steps (1 and 4) can't be reduced except by reducing the output capacitor's ESR. Fast regulator response can pull the output up more quickly after the initial step, but it can't

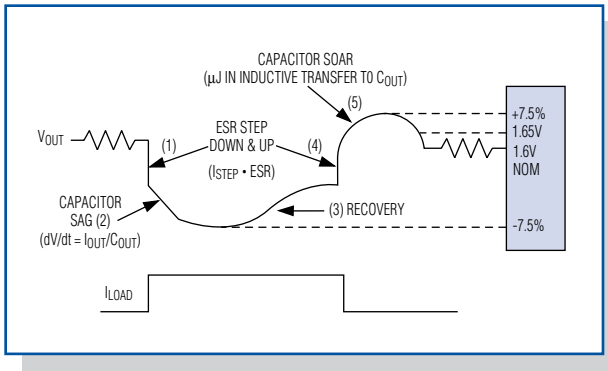



*Figure 1. This waveform illustrates the major components of a transient load step.*

stop the initial drop itself. Even the fastest DC-DC converter (the MAX1711, for example, which responds in less than 100ns) is too slow for the load transients instigated by CPU clocks running at 600MHz and above.

## Voltage positioning

It became clear that flogging a DC-DC converter for unrealistic transient behavior was hopeless. A 600MHz CPU generates 60 clock cycles during the MAX1711's 100ns response time. If the supply voltage *always* falls by $ESR_{COUT} \cdot I_{LOAD\ STEP}$ and stays there for several clock cycles, does it matter whether the output ever returns to its nominal value? From the CPU's standpoint, it doesn't matter. From the power supply's standpoint, however, it matters a lot.

The power supply much prefers that the voltage under load never returns to "nominal." That way, nearly twice as much transient voltage rise can be accommodated when the load is removed. Similarly, twice as much transient drop is allowed when the load is applied. **Figure 2** illustrates the different ways a voltage converter can respond to a load step.

These considerations have led to a new type of specification for CPU power supplies (see the gray box in Figure 1). The nominal voltage is 1.6V, but load-dependent droop can pull it down by 7.5% (quite sloppy by current CPU standards). It can also rise by 7.5% (short-term pulses only) when the load drops from full to zero. Output voltage in the steady state must not exceed 1.65V including noise and ripple. These numbers help minimize the capacitor count while allowing major gains in battery life and heat reduction.

To take full advantage of the wider limits for CPU power supplies, you can define a voltage/load profile for a given supply. This characteristic lets you implement a controlled form of load rejection—sometimes called voltage positioning—in which the output voltage is positioned as a function of load current. Voltage positioning allows the output to droop, and does not waste energy and money trying to prop it back up. Instead, the output is set to fall in a defined way as the load current increases. This approach offers a more graceful response to transient problems than the brute force approach (which offers limited benefits yet requires more capacitance and more speed from the DC-DC converter).

Voltage positioning capability can be added to many DC-DC controllers with no more than three resistors **(Figure 3)**. R4 and R5 add a small positive offset to the set output voltage, raising it from a nominal 1.6V (in this example) to 1.62V. R6 ($R_{VP}$) is in series with the output, matching the worst-case ESR of the output capacitor. The effect of $R_{VP}$ is to insert a defined, load-dependent voltage drop.

If $R_{VP}$ matches the filter capacitor's ESR, the output falls by the initial load-step drop ($ESR \cdot I_{LOAD}$), and remains at that level for as long as the load remains unchanged. Reducing the load causes the voltage level to rise by ($\Delta I \cdot ESR$). After a brief transient pulse from the last inductor discharge and before the controller's 100ns response (but within the allowed 7.5% limit), the DC level again remains at a level defined by the no-load voltage (1.62V in this case) minus $I_{LOAD} \cdot R_Z$. See **Figure 4**.

Adding 5mΩ in series with the output reduces efficiency. However, it also reduces the CPU's operating voltage under heavy load, which lowers power dissipation and improves battery life. Compared with conventional (nonpositioned) regulators, a voltage-positioned design lowers the CPU dissipation by 1.38W and lowers the overall power consumption by 0.4W **(Figures 5, 6)**.

## Effective efficiency

Because this improvement comes at the expense of conversion efficiency, it may be helpful to propose a new term that compares a voltage-positioned circuit with a conventional (nonpositioned) one. This term, "effective efficiency," is the efficiency required in a nonvoltage-positioned design to equal the performance of a voltage-positioned design.

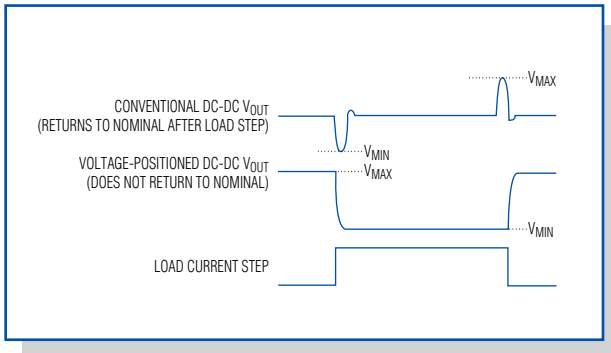
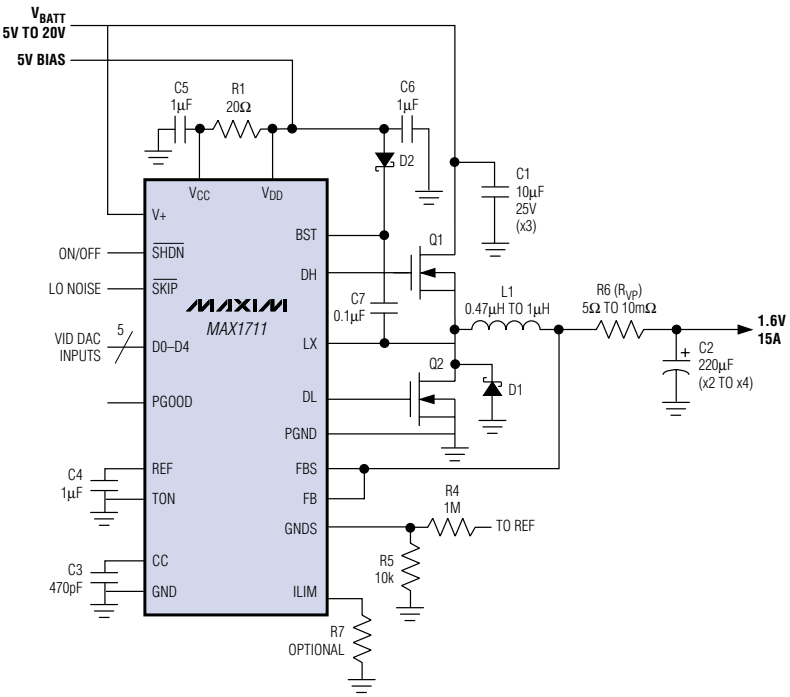



*Figure 2. Because voltage-positioned regulators don't attempt to restore the output voltage to a centered "nominal" after each load step, they allow larger transient excursions. This extra margin reduces power consumption and the output-capacitor count as well.*




| $I_{OUT}$(A) | C1(µF) | L1(µH) | R6($R_{VP}$, mΩ) | R7 | C2(µF) | Q1 | Q2 |
|---|---|---|---|---|---|---|---|
| 7 | (2) 10 | 1 | 10 | ($I_{LIM}$ = $V_{CC}$) | (2) 220 | IRF7807 | IRF7805 |
| 10 | (3) 10 | 0.68 | 8 | ($I_{LIM}$ = $V_{CC}$) | (3) 220 | IRF7811 | IRF7809 |
| 12 | (3) 10 | 0.47 | 7 | 220kΩ | (4) 220 | IRF7811 | IRF7809 |
| 15 | (4) 10 | 0.47 | 5 | 210kΩ | (4) 220 | IRF7811 | IRF7809* |

*C1 = Ceramic Capacitor, C2 = Panasonic SP series: EEFUEOE221R.*
**For continuous 15A load, use (2) IRF7811 or (2) IRF7805 due to thermal limitation of IR7809.*

*Figure 3. This efficient 15A regulated supply easily converts to a voltage-positioned design with the addition of three resistors: R4, R5, and R6 ($R_{VP}$).*

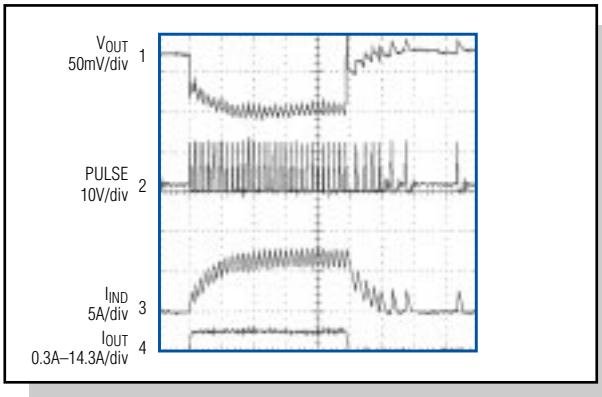



*Figure 4. The step response of Figure 3's circuit illustrates the advantage of a voltage-positioned output.*

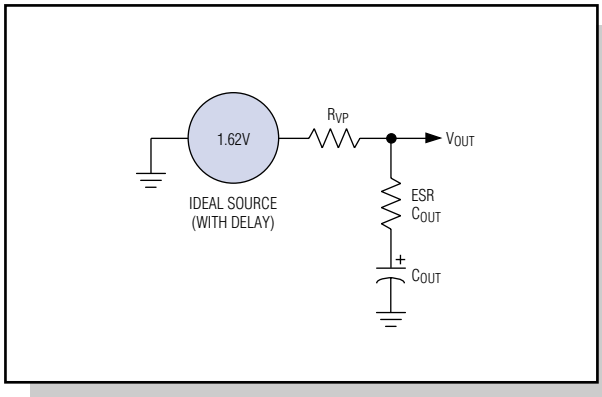



*Figure 5. This simplified model illustrates the basics of voltage positioning. The ideal "square-wave" voltage response to a load step (Figure 2) occurs when $R_{VP}$ equals ESR (the effective series resistance of $C_{OUT}$).*

To determine the effective efficiency of a voltage-positioned regulator, first measure its efficiency in the conventional way [($V_{OUT} \cdot I_{OUT}$)/($V_{IN} \cdot I_{IN}$)], then model the load as a resistance for each efficiency data point ($R_{LOAD} = V_{OUT}/I_{OUT}$). Next, calculate the output current for each $R_{LOAD}$ data point, using the nonpositioned output voltage ($I_{NP} = V_{NP}/R_{LOAD}$, where $V_{NP}$ = 1.6V in this case). Effective efficiency is then calculated at each $I_{NP}$ data point, as the nonpositioned power output ($V_{NP} \cdot I_{NP}$) divided by the measured voltage-positioned power input ($V_{OUT} \cdot I_{OUT}$). Note that an effective efficiency exceeding 100% is mathematically possible, but has yet to be achieved.

**Figure 7** shows how dramatic this improvement can be for a typical CPU power supply. To match the benefits derived from voltage positioning, a conventional design at full load would need an efficiency improvement of nearly 8%.

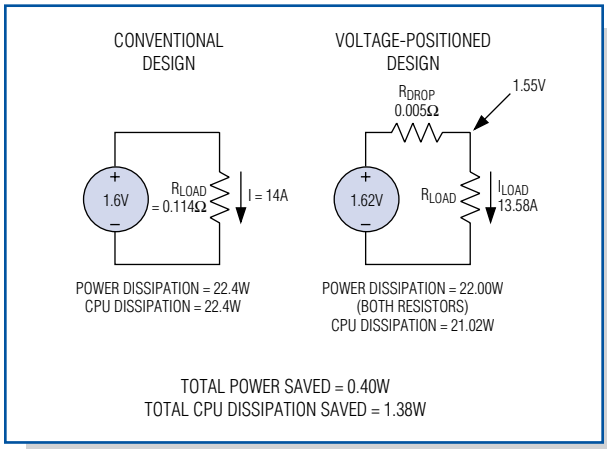



*Figure 6. Despite added output resistance that reduces the conversion efficiency, a voltage-positioned design reduces power dissipation in the power supply and within the CPU.*

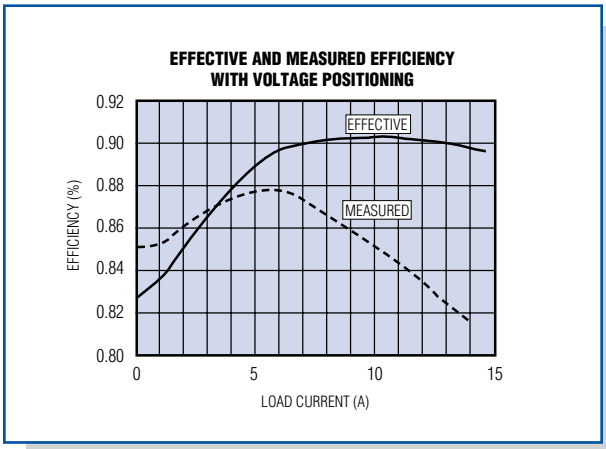



*Figure 7. These plots show an 8% advantage for the voltage-positioned CPU power supply at full load. A conventional design would need 90% conversion efficiency to match the 82% efficiency of a voltage-positioned design delivering 14A.*

# Statistical confidence levels for estimating error probability

*Many components in digital communication systems must meet a minimum specification for the probability of bit error (P(ε)). For a given system, P(ε) can be estimated by comparing the output bit pattern with a predefined pattern applied to the input. Any discrepancy between the input and output bit streams is flagged as an error, and the ratio of detected bit errors (ε) to total bits transmitted (n) is P′(ε), where the prime character signifies an estimate of the actual P(ε). The quality of this estimate improves with the total number of bits transmitted. The relationship can be expressed as*

$$P'(\varepsilon) = \frac{\varepsilon}{n} \xrightarrow[n \to \infty]{} P(\varepsilon) \quad \text{[eq. 1]}$$

It is important to transmit enough bits through the system to ensure that P′(ε) is a reasonable approximation of the actual P(ε) (i.e., the value to be obtained if the test could proceed for an infinite amount of time). For a reasonable limit on test time, therefore, we must know the minimum number of bits that yields a statistically valid test.

In many cases, we must verify only that P(ε) is at least as good as some predefined standard. In other words, it is sufficient to prove that P(ε) is less than some upper limit. For example, the P(ε) required in many telecommunication systems is $10^{-10}$ or better (an upper limit of $10^{-10}$). The statistical idea of associating a *confidence level* with an upper limit can be used to postulate, with quantifiable confidence, that the actual P(ε) is less than the specified limit. As a primary advantage, this method lets you trade test time for measurement accuracy.

## Defining the statistical confidence level

The statistical confidence level is defined as the probability, based on a set of measurements, that the actual probability of an event is better than some specified level. (For the purpose of this definition, actual probability means the probability that is measured in the limit as the number of trials tends toward infinity.) When applied to P(ε) estimation, the definition of statistical confidence level can be restated as the probability (based on ε detected errors out of n bits transmitted) that the actual P(ε) is better than a specified level γ (such as $10^{-10}$). Mathematically, this can be expressed as

$$CL = P\left[P(\varepsilon) < \gamma \,\middle|\, \varepsilon, n\right] \quad \text{[eq. 2]}$$

where P[ ] indicates probability and CL is the confidence level. Because confidence level is a probability by definition, the possible values range from 0% to 100%.

After computing the confidence level, we can say we have CL percent confidence that the P(ε) is better than γ. As another interpretation, if we repeat the bit-error test many times and recompute P′(ε) = ε/n for each test period, we expect P′(ε) to be better than γ for CL percent of the measurements.

## Calculating the confidence level

Calculations of the confidence level are based on the binomial distribution function described in many statistics texts[1,2]. The binomial distribution function is generally written as

$$P_n(k) = \binom{n}{k} p^k q^{n-k}, \text{ where } \binom{n}{k} \text{ is defined as } \frac{n!}{k!(n-k)!} \quad \text{[eq. 3]}$$

Equation [3] gives the probability that k events (i.e., bit errors) occur in n trials (i.e., n bits transmitted), where p is the probability of event occurrence in a single trial (i.e., a bit error), and q is the probability that the event does not occur in a single trial (i.e., no bit error). Note that the binomial distribution models events that have two possible outcomes, such as success/failure, heads/tails, or error/no error. Thus, p + q = 1.

When we are interested in the probability that N or fewer events occur in n trials (or, conversely, that greater than N events occur), then the cumulative binomial distribution function of Equation 4 is useful:

$$P(\varepsilon \le N) = \sum_{k=0}^{N} P_n(k) = \sum_{k=0}^{N} \left( \frac{n!}{k!(n-k)!} \right) p^k q^{n-k}$$

$$P(\varepsilon > N) = 1 - P(\varepsilon \le N) = \sum_{k=N+1}^{n} \left( \frac{n!}{k!(n-k)!} \right) p^k q^{n-k} \quad \text{[eq. 4]}$$

Graphical representations of Equations 3 and 4, along with some of their properties, are summarized in **Figure 1**.

## Binomial distribution function

In a typical confidence-level measurement, we start by choosing a satisfactory level of confidence and hypothesizing a value for p (the probability of bit error in transmitting a single bit). We represent the chosen p value as $p_h$. In general, we choose these values according to a limit imposed by specification (e.g., if the specification is $P(\varepsilon) \leq 10^{-10}$, we choose $p_h = 10^{-10}$ and a confidence level of, say, 99%).

We can then use Equation 4 to determine the probability $P(\varepsilon > N|p_h)$, based on $p_h$, that more than N bit errors will occur when n total bits are transmitted. If, during actual testing, less than N bit errors occur (even though $P(\varepsilon > N|p_h)$ is high), then one of two conclusions can be made: (a) we just got lucky, or (b) the actual value of p is less than $p_h$. If we repeat the test over and over and continue to measure less than N bit errors, then we become more and more confident in conclusion (b).

The quantity $P(\varepsilon > N|p_h)$ defines our level of confidence in conclusion (b). If $p_h = p$, we have a high probability of detecting more bit errors than N. When we measure less than N errors, we conclude that p is probably less than $p_h$, and we define as the confidence level this probability that our conclusion is correct. In other words, we are CL% confident that $P(\varepsilon)$ (the actual probability of bit error) is less than $p_h$.

In terms of the cumulative binomial distribution function, the confidence level is defined as

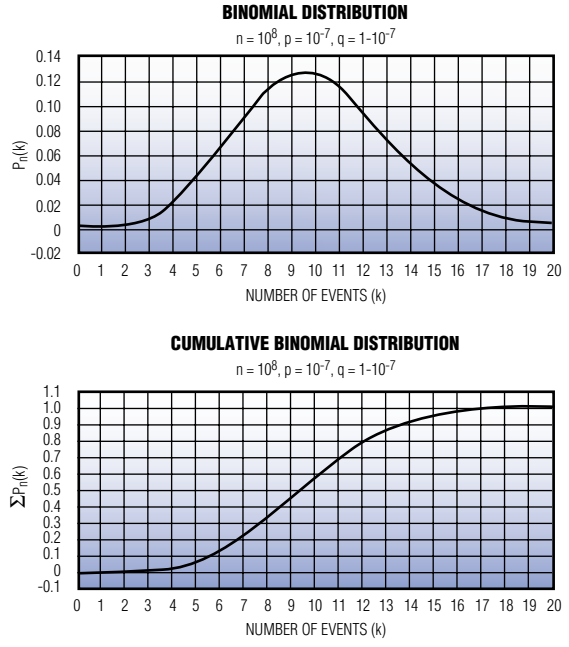
$$CL = P\left(\varepsilon > N \mid p_h\right) = 1 - \sum_{k=0}^{N} \left(\frac{n!}{k!(n-k)!}\right)(p_h)^k (1-p_h)^{n-k} \quad \text{[eq. 5]}$$

where CL is the confidence level in terms of percent.

As noted above, when using the confidence-level method we generally choose a hypothetical value of p ($p_h$) along with a desired confidence level (CL), and then solve Equation 5 to determine how many bits (n) we must transmit through the system (with N or fewer errors) to prove our hypothesis. Solving for n and N can prove difficult unless approximations are made.

If np > 1 (i.e., we transmit at least as many bits as the mathematical inverse of the bit error rate), and k has the same order of magnitude as np, then the Poisson theorem[1] (Equation 6) provides a conservative estimate of the binomial distribution function:

$$P_n(k) = \left(\frac{n!}{k!(n-k)!}\right) p^k q^{n-k} \xrightarrow[n\to\infty]{} \frac{(np)^k}{k!} e^{-np} \quad \text{[eq. 6]}$$




$$P_n(k) = \left(\frac{n!}{k!(n-k)!}\right) p^k q^{n-}$$

n = Total number of trials
(i.e., total bits transmitted)

k = Number of events occurring in
n trials (i.e., bit errors)

p = Probability that an event occurs in
one trial (i.e., probability of bit error)

q = Probability that an event does not occur in
one trial (i.e., probability of no bit error)

p + q = 1
Mean ($\mu$) = nq
Variance ($\sigma^2$) = npq

$$CL = 1 - \sum_{k=0}^{N} P_n(k)$$

*Figure 1. The binomial and cumulative binomial distributions relate number of trials and measured error to the probabilities that an error will (or will not) occur.*

Equation 7 shows how Equation 6 can be used to obtain an approximation for the cumulative binomial distribution as well:

$$\sum_{k=0}^{N} P_n(k) \approx \sum_{k=0}^{N} \frac{(np)^k}{k!} e^{-np} \quad \text{[eq. 7]}$$

We can combine Equations 5 and 7, and solve for n as follows:

$$\sum_{k=0}^{N} P_n(k) = 1 - CL \quad \text{(by rearranging Equation 5)}$$

$$\sum_{k=0}^{N} \frac{(np)^k}{k!} e^{-np} = 1 - CL \quad \text{(using Equation 7)}$$

$$-np = \ln\left[\frac{1-CL}{\sum_{k=0}^{N} \frac{(np)^k}{k!}}\right] \qquad n = -\frac{\ln(1-CL)}{p} + \frac{\ln\left(\sum_{k=0}^{N} \frac{(np)^k}{k!}\right)}{p}$$

[eq. 8]

Note that the second term in Equation 8 equals zero for N = 0, and for that case the equation is easily solved. Solutions to Equation 8 are more difficult for N > 0, but they can be obtained empirically, using a computer. We can now determine the total number of bits that must be transmitted through the system to achieve a desired confidence level. Following is an example of this procedure:

1) Select $p_h$, the hypothetical value of p. This value is the probability of bit error that we would like to verify. For example, if we want to show that $P(\varepsilon) \le 10^{-10}$, then we set p in Equation 8 equal to $p_h = 10^{-10}$.
2) Select the desired confidence level. Here we are forced to trade confidence for test time. To minimize test time, choose the lowest reasonable confidence level. The trade-off between test time and confidence level is proportional to -ln(1 - CL). See **Figure 2**.
3) Solve Equation 8 for n. In most cases, this task is simplified by assuming that no bit errors will occur during the test (i.e., N = 0).
4) Calculate the test time. The time required to complete the test is n/R, where R is the data rate.

## Using CL to estimate P(ε)

Many telecommunication systems specify $10^{-10}$ or better for P(ε). Assume that we must test two clock/data-recovery chips, the MAX3675 (622Mbps) and the MAX3875 (2.5Gbps), to verify compliance with this specification. We first set $p_h = 10^{-10}$. We would like a test that yields 100% confidence in the desired specification, but that requires an infinite test time. We therefore settle for a confidence level of 99%. Next we solve Equation 8 for n using various values of N (0, 1, 2, 3, etc.). The results are shown below in **Table 1**.

From Table 1 we see that if no bit errors are detected for 18.5s (in a 2.5Gbps system), then we have a 99% confidence level that $P(\varepsilon) \le 10^{-10}$. If one bit error occurs in 26.7s of testing, or two bit errors in 33.7s, the result is the same: a 99% confidence level that $P(\varepsilon) \le 10^{-10}$.

To develop a standard P(ε) test for the MAX3675/MAX3875, we might select the test time corresponding to N = 3 from Table 1. Using a bit-error-rate tester (BERT), we transmit $10^{11}$ bits through each of the two chips. The test time for $10^{11}$ bits is 2min 41s at 622Mbps, or 40.2s at 2.5Gbps. At the end of the test time, we check the number of detected bit errors (ε). If ε ≤ 3, the device has passed and we are 99% confident that $P(\varepsilon) \le 10^{-10}$.

## Stressing the system to reduce test time

Dan Wolaver has documented a method for reducing test time by stressing the system[3]. It is based on an assumption that the dominant cause of bit errors is thermal (Gaussian) noise at the input of the receiver. (Note that this assumption excludes jitter and other potential causes of error.) For systems in which this assumption is valid, the signal-to-noise ratio (SNR) can be reduced by inserting a fixed attenuation in the transmission path (i.e., the attenuation applies to the signal only; not the dominant noise source). In the previous example (MAX3675 and MAX3875), it was determined that jitter

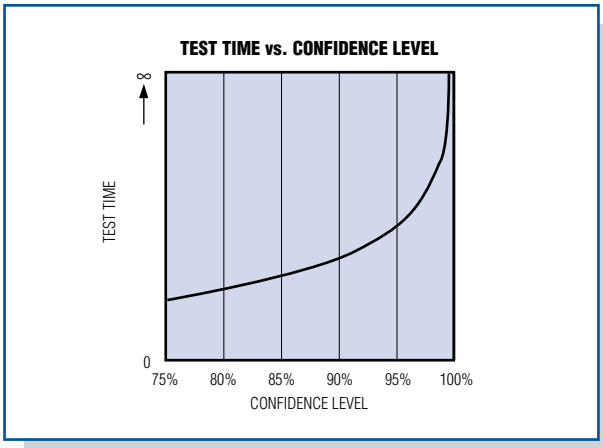



*Figure 2. Confidence level (in a specified error rate) rises with the allowed test time.*

**Table 1. Estimation of Bit Error Probability (Example: CL = 99% and $p_h = 10^{-10}$)**

| Bit Errors ≤ N<br>N = | Required Number of Bits to Transmit (n) | Test Time for Bit Rate of 622Mbps (seconds) | Test Time for Bit Rate of 2.5Gbps (seconds) |
|---|---|---|---|
| 0 | $4.61 \cdot 10^{10}$ | 74.1 | 18.5 |
| 1 | $6.64 \cdot 10^{10}$ | 106 | 26.7 |
| 2 | $8.40 \cdot 10^{10}$ | 135 | 33.7 |
| 3 | $1.00 \cdot 10^{11}$ | 161 | 40.2 |
| 4 | $1.16 \cdot 10^{11}$ | 186 | 46.6 |

effects and nonlinear gain in the input limiting amplifier violated the key assumptions of this method, so it was not employed.

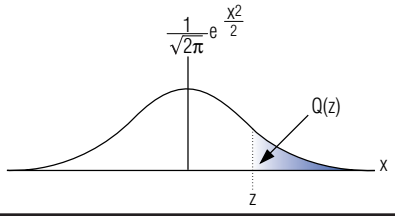
In systems where the assumption is valid, the probability of bit error can generally be calculated[4, 5] as:

$$P(\varepsilon) = Q\left(\frac{\sqrt{SNR_{electrical}}}{2}\right) = Q\left(\frac{\sqrt{SNR_{optional}}}{2}\right) \quad \text{[eq. 9]}$$

where Q(x) is the complementary error (or the "Q" function included in many communications textbooks[6]. A variety of other sources for this data are available, including the NORMDIST function in Microsoft Excel. Key values for the complementary error function are listed in **Table 2**.

**Table 2. Tabulated Values for the Complementary Error ("Q") Function**

| $z = \frac{x-\mu}{\sigma}$ | $Q(z) = \frac{1}{\sqrt{2p}} \int_z^{\infty} e^{\frac{x^2}{2}}\, dx$ |
|---|---|
| 3.71 | $10^{-4}$ |
| 4.26 | $10^{-5}$ |
| 4.75 | $10^{-6}$ |
| 5.19 | $10^{-7}$ |
| 5.61 | $10^{-8}$ |
| 5.99 | $10^{-9}$ |
| 6.36 | $10^{-10}$ |
| 6.70 | $10^{-11}$ |
| 7.03 | $10^{-12}$ |




Equation 9 shows that the probability of bit error increases as the SNR decreases. If a fixed attenuation ($\alpha$) is inserted in the transmission path, then the signal power ($P_S$) is reduced by the factor $\alpha$ while the noise power ($P_N$) is unchanged. The SNR is therefore reduced from $SNR = P_S/P_N$ to $SNR = P_S/\alpha P_N$. The corresponding $P(\varepsilon)$ is increased by a factor that can be calculated using Equation 9 and Table 2.

We can now repeat the earlier test method using a modified value for $p_h$. The calculation can then be extrapolated to any other SNR by using Equation 9. The result is the same, but the test time may be significantly shorter.

The disadvantage of stressing a system is that measurements and calculations must be carried out with more precision, because extrapolating the results to their non-stressed levels multiplies the errors due to roundoff truncation, measurement tolerance, etc.

## References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# NEW PRODUCTS

## 8-bit ADC with on-chip T/H converts at 1.5Gsps

The MAX108 is an 8-bit monolithic, bipolar analog-to-digital converter (ADC) with a digitizing rate of 1.5Gsps. By enabling direct IF sampling in broadband, high-rate receivers employing PSK or QAM modulation, the MAX108 is an excellent choice for digital communications where ultra-high sampling rates, wide bandwidth, and high-level dynamic performance are required.

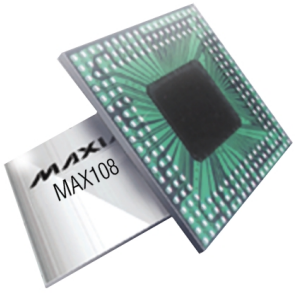
This is the first 8-bit, 1.5Gsps monolithic ADC to achieve a 47dB SINAD (typ) and 54dB SFDR at twice the Nyquist input frequency (1.5GHz), and a full 47dB SINAD and 54dB SFDR at the Nyquist input frequency of 750MHz. (The closest competitor specifies a typical 42dB SINAD and 45dB SFDR at 1.0GHz—twice the Nyquist input frequency for that device.)

The MAX108 achieves high performance through innovative design and the use of Maxim's proprietary 27GHz bipolar-IC process. An integrated, fully differential input track/hold (T/H) combined with precision laser-trimmed resistors produces typical INL and DNL errors less than ±0.25LSB, a full-power bandwidth of 2.2GHz, and less than 0.5ps aperture jitter. A proprietary on-chip decoding scheme further enhances performance by ensuring a low occurrence of metastable states, with no error exceeding 1LSB.

To simplify the digital interface, an internal, selectable 8:16 output demultiplexer slows the 1.5Gsps data rate to 750 megawords per second, ported to two parallel, differential 8-bit, low-voltage (PECL) outputs. The MAX108 also supports single-port operation at lower sampling rates. It presents data in offset-binary format, and includes an output clock and overrange bit. It operates from ±5V, and supports an output interface in the +3V to +5V range.

Proper packaging is critical to achieving good performance at these frequencies. A 25mm x 25mm x 1.2mm, 192-contact Enhanced Super Ball-Grid Array (ESBGA™) package minimizes parasitic effects, provides controlled-impedance signal paths, and eliminates the need for heatsinking in most applications. The MAX108 allows easy performance upgrades from the pin-compatible MAX104 (1Gsps), and MAX106 (600Msps) ADCs. Contact factory for availability. An evaluation kit including the MAX108 is recommended (MAX108EVKIT, $850.00).

*ESBGA is a trademark of Amkor/Anam.*




## 12-bit multichannel ADCs feature parallel I/O and QSOP packages

The MAX1290–MAX1297 ADCs offer a parallel interface and 12-bit resolution. Their low cost, small footprint, and high sample rates (to 420ksps) set new standards for parallel-I/O, 12-bit ADCs. Ideal for portable data-acquisition and battery-powered applications, these devices offer an internal reference, 8- and 12-bit interface options, +3V or +5V single-supply operation, and multiple input channels (2, 4, 6, or 8).

The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation. The full-scale analog input range can be set by either the internal reference (2.5V) or an external reference in the 1V to $V_{DD}$ range.

All devices operate from a single +3V or +5V analog supply. They consume only 1.5mA at 100ksps sample rates, and at lower rates a software power-down mode reduces the supply current to below 10µA. The MAX1290–MAX1293 feature an 8-bit-parallel I/O, and the MAX1294–MAX1297 feature a 12-bit-parallel I/O. Thanks to a $V_{LOGIC}$ pin, the MAX1290–MAX1293 are the only ADCs able to interface directly with digital supplies in the +1.8V to +5V range.

The MAX1290–MAX1297 are available in 24-pin and 28-pin QSOP packages, with prices starting at $5.60 (1000-up, FOB USA).

## 10-/12-bit $V_{OUT}$ DACs feature serial interface

The 12-bit MAX5302 and 10-bit MAX5304 digital-to-analog converters (DACs) each combine a low-power voltage-output DAC and precision output amplifier in a tiny 8-pin µMAX package. They operate on a single +5V supply, draw less than 280µA of operating supply current, and draw only 2µA in shutdown.

The output amplifier's inverting input enables the user to configure the device for specific gain configurations, remote sensing, and high output-current capability. This flexibility, along with a software shutdown and power-on reset (which clears the DAC output to zero), makes these devices suitable for a wide range of applications including industrial process control.

Each device has a serial interface compatible with the SPI™, QSPI™, and MICROWIRE™ serial-data standards. The DAC's double-buffered input consists of an input register followed by a DAC register.

Sixteen-bit serial words load data into the input register, and the DAC register can be updated either simultaneously with the input register or independently. To allow a direct interface with optocouplers, all logic inputs are TTL/CMOS compatible and buffered with a Schmitt trigger.

The MAX5302/MAX5304 come in 8-pin µMAX packages, with prices starting at $1.75 (1000-up, FOB USA).

*SPI and QSPI are trademarks of Motorola, Inc.*

*MICROWIRE is a trademark of National Semiconductor Corp.*

# NEW PRODUCTS

## 1.8V nanopower comparator/ references in tiny SOT23-5

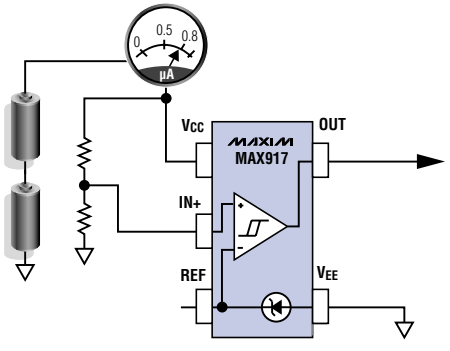
The MAX917–MAX920 nanopower comparators are guaranteed to operate from a single supply down to +1.8V while drawing a stingy 380nA. The MAX918/MAX919 devices, with an additional 1.245V ±1.5% voltage reference, still draw only 750nA of supply current. Their small footprint, Rail-to-Rail® I/O, and nanopower operation from two cells make these devices ideal for all battery monitoring and battery management in portable applications.

All four devices feature Beyond-the-Rails™ inputs and rail-to-rail outputs. Unique design in the output stage limits supply-current surges while switching. This proprietary architecture virtually eliminates the supply-current glitches typical of many other comparators, and maintains low overall power consumption under dynamic conditions.

The MAX917/MAX919 have a push-pull output stage that sinks and sources current. The MAX918/MAX920 have an open-drain output stage that can be pulled beyond $V_{CC}$, making them suitable for mixed-voltage designs. The MAX917–MAX920 are offered in 5-pin SOT23 and 8-pin SO packages. Prices start from $0.66 (1000-up, FOB USA).

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

*Beyond-the-Rails is a trademark of Maxim Integrated Products.*




## Micropower amps offer 54 fixed-gain versions

The MAX4074/MAX4075 single/dual, micropower, GainAmps™ deliver fixed gains through internal gain-setting resistors. By replacing an amplifier and two resistors with a single 5-pin SOT23 package (3mm x 3mm), these amplifiers offer a choice of 27 inverting and 27 noninverting factory-trimmed gains. Applications such as ADC amplifiers and Sallen-Key filters benefit from the GainAmps' excellent resistor matching, which minimizes the size and cost of circuit layouts while providing 0.1% total gain accuracy.

The MAX4074/MAX4075 provide 27 inverting gains (from -0.25V/V to -100V/V) and 27 noninverting gains (from +1.25V/V to +101V/V). They operate from a single supply voltage in the +2.5V to +5.5V range. By optimizing frequency compensation, the high-gain versions achieve gain-bandwidth (GBW) products as high as 3MHz, while drawing only 34µA supply current. They also feature high-voltage input fault protection without excessive current draw, which allows operation with either input voltage as high as ±17V. The outputs can swing rail-to-rail and maintain DC accuracy while driving 10kΩ loads. Each amplifier is stable for capacitive loads up to 500pF.

The single, micropower, fixed-gain amplifier (MAX4074) is available in the 5-pin SOT23 package. The dual amplifier (MAX4075) is available in space-saving 8-pin µMAX and SO packages. Prices start from $0.68 (1000-up, FOB USA).

*GainAmps is a trademark of Maxim Integrated Products.*

## 10V/µs op amp with rail-to-rail I/O fits tiny SC70 package

The 10V/µs MAX4490 op amp comes in a miniature 5-pin SC70 package, which measures only 2mm x 2.1mm and occupies less than half the board area of a SOT23-5.

Rail-to-rail inputs and output increase flexibility and dynamic range, and simplify the circuit design for applications powered from a single +2.7V to +5.5V supply. The combination of fast slew rate, miniature packaging, and low-voltage operation makes this op amp ideal for portable applications ranging from audio amplifiers to the control of RF power amplifiers.

The MAX4490 achieves a 10MHz GBW product while drawing only 800µA of supply current. Other features include a low 50pA input bias current and a 2kΩ drive. Sample/hold and ADC-predriver circuits benefit from the 200pF capacitive load-driving capability.

The MAX4490 is available in the space-saving 5-pin SOT23 package as well as the ultra-small 5-pin SC70 package. Prices start from $0.55 (1000-up, FOB USA).

## Low-distortion differential line receivers slew 5000V/µs

The MAX4444/MAX4445 are 550MHz, low-distortion, differential-to-single-ended line receivers. Their combination of wide bandwidth, -60dB SFDR (spurious-free dynamic range) at 5MHz, 5000V/µs slew rate, and low noise make these line receivers ideal for high-speed cable testers and a variety of other wideband communications applications. They also have 0.1dB gain flatness to 80MHz, and deliver output currents to 120mA.

For high-speed video and RF signal processing, these devices offer low differential gain/phase error (0.07%/0.05°) and low noise (25nV/$\sqrt{Hz}$). The MAX4445 has an internally fixed gain of +2V/V. The MAX4444 can be externally set for gains greater than or equal to +2V/V. In addition, both devices offer a low-power disable mode that reduces supply current to 3.5mA.

Both are available in 16-pin SO packages, with prices starting at $1.95 (1000-up, FOB USA).

# NEW PRODUCTS

## Low-distortion differential line drivers slew 6500V/µs

The MAX4447/MAX4448/MAX4449 are 430MHz, low-distortion, single-ended-to-differential line drivers. Combining wide bandwidth, -78dB SFDR at 5MHz, slew rates up to 6500V/µs, and differential outputs that swing ±6.2V into 50Ω, these line drivers are ideal for use in wideband communications, including high-speed cable testers. They offer 0.1dB gain flatness to 200MHz and output-current capability to 130mA.

For high-speed video and RF signal-processing applications, these devices offer low differential gain/phase error (0.01%/0.02°) and low noise (24nV/$\sqrt{Hz}$). The MAX4447 has an internally fixed gain of +2V/V. The MAX4448/MAX4449 allow external settings of gain greater than or equal to +2V/V and +5V/V, respectively. In addition, all devices offer a low-power disable mode that reduces the supply current to 5.5mA.

These line drivers are offered in 16-pin SO packages, with prices starting at $2.05 (1000-up, FOB USA).

## 210MHz single-supply op amp in ultra-small SC70 package

The MAX4450 is a 210MHz, low-power, single-supply op amp that fits in an ultra-small SC70 package (half the size of a SOT23-5). Its single-supply operation, rail-to-rail outputs, and wide bandwidth make it ideal for wideband consumer applications such as set-top boxes, surveillance video systems, digital cameras, and CD-ROM drives.

The MAX4450 operates from a single +4.5V to +11V supply, or dual ±2.25V to ±5.5V supplies. Drawing only 6.5mA of quiescent supply current, it achieves a -3dB bandwidth of 210MHz, slew rates to 485V/µs, and an output current drive of ±80mA.

The MAX4450 offers 0.1dB gain flatness to 55MHz, low differential gain/phase errors of 0.02%/0.08°, and an SFDR of -65dBc at 5MHz. Its input common-mode range includes ground and the output swings rail-to-rail, suiting the device for low-voltage, single-supply applications. The MAX4450 comes in both 5-pin SC70 and SOT23 packages, with prices starting at $0.54 (50,000-up, FOB USA).

## Precision dual high-speed switches have 5Ω on-resistance

The MAX4621/MAX4622/MAX4623 switches are precision, dual, high-speed analog devices. On-resistances are 5Ω max, matched within a device to within 0.5Ω max and flat to within 0.5Ω max over the specified signal range. Each switch handles rail-to-rail analog signals and exhibits low off-channel leakage currents: <500pA at +25°C, and only 5nA max at +85°C. Fast switching times include turn-on <250ns and turn-off <200ns.

These switches are ideal for low-distortion applications, and are preferred over mechanical relays in automated test equipment (ATE) and current-switching applications because they require less space, are more reliable, and operate with much less power.

The SPST MAX4621 and DPST MAX4623 switches are normally open (NO), and the SPDT MAX4622 has two NO and two normally closed (NC) poles. All devices guarantee break-before-make switching. They operate from a single +4.5V to +36V supply, or from dual ±4.5V to ±18V supplies. A dedicated logic-supply pin ($V_L$) enables compatibility with TTL/CMOS logic across the entire supply-voltage range.

These switches are pin compatible with DG401/DG403/DG405 switches and come in 16-pin plastic DIP and narrow-SO packages. Prices start at $1.53 (1000-up, FOB USA).

## Circuit protector withstands ±36V overvoltages

The MAX4505 single-channel circuit protector withstands up to ±36V with power on, and ±40V with power off. The input terminal becomes open-circuited during a fault condition, allowing only nanoamperes of leakage current from the source, and the output is able to deliver as much as 19mA (with proper polarity of supply voltage) to the load. The resulting rail-to-rail output is unambiguous from beginning to end of the fault.

The MAX4505 operates with unipolar (+9V to +36V) or bipolar (±8V to ±18V) power supplies. It features low on-resistance (100Ω max) and no logic-control inputs (the device is always on when supply voltage is present). It is available in a tiny 5-pin SOT23 or 8-pin µMAX package, with prices starting at $0.83 (1000-up, FOB USA).

## Quad switches feature 10Ω on-resistance

The MAX4614/MAX4615/MAX4616 are low-voltage, low-on-resistance quad analog switches. Each device operates from a single supply voltage in the +2.0V to +5.5V range, and features low on-resistance (10Ω max) at 5V. The MAX4614 is pin compatible with the industry-standard 74HC4066 and CD4066 switches.

Fast switching times of 12ns $t_{ON}$, 10ns $t_{OFF}$ at +25°C make these devices ideal for use in high-speed data-acquisition systems and communications circuits. Each guarantees matching and flatness to 1Ω max. All digital inputs have +0.8V logic thresholds, ensuring compatibility with TTL and CMOS logic when using a +5V power supply.

The MAX4614 has four normally open (NO) switches, and the MAX4615 has four normally closed (NC) switches. The MAX4616 has two NO and two NC switches. All are available in space-saving 14-pin TSSOP, SO, and DIP packages. Prices start from $0.80 (1000-up, FOB USA).

# NEW PRODUCTS

## Quad and dual SPST CMOS analog switches have 2.5Ω/5Ω $R_{ON}$

The MAX4661–MAX4669 SPST CMOS analog switches feature low on-resistance, matched to within 0.5Ω max and flat to within 0.5Ω max over the specified signal range. Each switch handles rail-to-rail analog signals, and the off-channel leakage current at +85°C is only 5nA max.

These devices are available as 2.5Ω max quad switches, 5Ω max quad switches, and 2.5Ω max dual switches. They are ideal for low-distortion applications, and are preferred over mechanical relays in ATE and current-switching applications because they are more reliable, require less space, and operate with much less power.

The MAX4661/MAX4664/MAX4667 have two normally closed (NC) switches, the MAX4662/MAX4665/MAX4668 have two normally open (NO) switches, and the MAX4663/MAX4666/MAX4669 (which guarantee break-before-make switching) have one NC and one NO switch. All operate from a single supply in the +4.5V to +36V range, or from dual supplies in the ±4.5V to ±20V range. A dedicated logic-supply pin ($V_L$) enables compatibility with TTL/CMOS logic across the entire supply-voltage range.

For even lower $R_{ON}$ (1.25Ω matched to within 0.3Ωmax and flat to within 0.3Ωmax), see the MAX4680/MAX4690/MAX4700 (dual SPST) data sheet.

The MAX4661–MAX4669 switches come in 16-pin SSOP, plastic DIP, narrow SO, and wide SO packages. Prices start at $1.91 (1000-up, FOB USA).

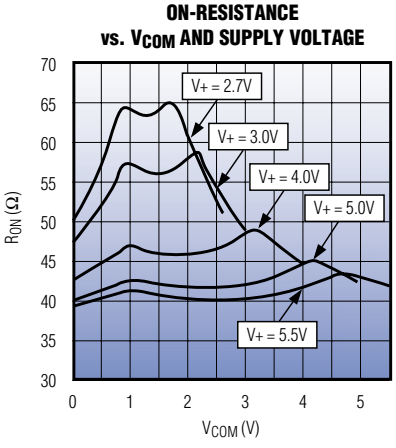
## Tiny multimedia switches feature -80dB off-isolation

The MAX4584–MAX4587 serial-interface switches and multiplexers have an excellent frequency response, suitable for use in high-performance audio/video applications. For audio to 20kHz, off-isolation is -80dB and crosstalk is -77dB. For video to 10MHz, off-isolation is -68dB and crosstalk is -70dB.

These products operate from a single +2.7V to +5.5V supply, and feature a low 65Ω max on-resistance at 5V. The channels are flat to within 5Ω and matched between channels to within 4Ω.

The MAX4584/MAX4585 each contain one single-pole/single-throw (SPST) switch and one single-pole/double-throw (SPDT) switch, both normally open (NO). The MAX4586/MAX4587 are configured as 4-to-1 multiplexers. The MAX4584/MAX4586 have a 2-wire, $I^2C$-compatible serial interface, and the MAX4585/MAX4587 have a 3-wire, SPI/QSPI/MICROWIRE-compatible interface.

These devices are available in tiny 10-pin µMAX packages, with prices starting at $1.12 for the MAX4584/MAX4585 and $1.26 for the MAX4586/MAX4587 (1000-up, FOB USA).




## High-speed step-down controller powers notebooks

The MAX1714 PWM controller provides the high efficiency, excellent transient response, and accurate DC output (1% over line and load) required for stepping down high battery voltage to the low supply voltages needed to power the CPU core and chipset/RAM sections of a notebook computer.

Maxim's proprietary quick-response, constant-on-time control scheme (Quick-PWM™) maintains a relatively constant switching frequency while handling wide ratios of input/output voltage with ease, and provides a 100ns "instant-on" response to load transients. By eliminating the current-sense resistor found in traditional current-mode PWMs, the MAX1714 achieves high efficiency at a reduced cost. Its capability for driving very large synchronous-rectifier MOSFETs further enhances efficiency.

By stepping down high battery voltage directly, the MAX1714's single-stage buck conversion achieves the highest possible efficiency. As an alternative, a two-stage conversion (stepping down the +5V supply instead of the battery) lets you minimize physical size.

The MAX1714 generates regulated supply voltages (CPU core, chipset, DRAM) as low as 1V. (For applications requiring VID compliance or DAC control of the output voltage, consider the MAX1710/MAX1711. For dual output voltages, consider the MAX1715.) Select the MAX1714A (in 20-pin QSOP with overvoltage protection) or the MAX1714B (in a 16-pin QSOP with no overvoltage protection). Prices start at $2.65 (1000-up, FOB USA).

*Quick-PWM is a trademark of Maxim Integrated Products.*

# NEW PRODUCTS

## Next-generation current-limited USB switches

The MAX1693, MAX1694, MAX893L, and MAX1607 represent the next generation of current-limited power switches for PCMCIA cards, the Universal Serial Bus (USB), and other Hot Swap™, plug-in applications. These switches prevent system crashes due to overcurrent or short-circuit conditions at the USB port. They offer the lowest cost and highest accuracy available for current-limiting applications.

The MAX1693/MAX1694 guarantee 1A max for current drawn from the system power supply. Compare this to the ±50% current-limit accuracy for polyfuses and other silicon devices; their worst-case continuous current can exceed 2A, requiring a larger and more expensive power supply. Even if a MAX1693/MAX1694 output is shorted, however, the foldback scheme reduces their switch current to only 500mA.

The MAX1693/MAX1694 generate a FAULT signal in response to a current limit, thermal shutdown, or undervoltage lockout. Their internal 10ms blanking period prevents brief, high-current transients from causing the FAULT pin to go low. If an overcurrent condition continues beyond 10ms, the MAX1693 sets FAULT low until the overcurrent is removed. The MAX1694 further protects the system power supply by latching FAULT low and turning off the power switch. Cycling the MAX1694 from off to on resets the switch. These switches are available in a space-saving 10-pin µMAX package (half the size of the 8-pin SO).

The MAX1607 has the same die and specifications as the MAX1693, but it is a pin-compatible upgrade to the TPS2014/TPS2015/TPS2041. The MAX893L lacks the 10ms fault-blanking feature, but offers a lower cost, pin-compatible upgrade to the earlier MAX890L.

Quiescent current in the on state is a low 14µA for all parts, and drops to only 0.1µA in the off state. Thermal overload protection automatically limits the power dissipation and junction temperature to safe levels. Prices start at $0.80 (1000-up, FOB USA).

*Hot Swap is a trademark of Linear Technology Corp.*

## Complete Li+ battery charger fits in handset

The MAX1679, when combined with an external P-channel MOSFET, forms a complete stand-alone charger for single-cell lithium-ion (Li+) batteries. The result is a tiny circuit whose power dissipation (virtually zero) minimizes heating in the phone handset. It determines the charge-termination voltage with accuracy better than 0.75%.

For safety, the MAX1679's internal timer provides a selectable charger timeout. To prevent charging when the battery is too hot or cold, an optional thermistor monitors the temperature continuously.

Other features include a low-current precharge for conditioning cells that are nearly dead, and a pulsed top-off charge that achieves full-battery capacity with each complete charge cycle. An inexpensive current-limited wall cube sets the charging current. When the wall cube is removed, the MAX1679 automatically powers down and draws less than 1µA from the battery.

The MAX1679's open-drain CHG output can drive an external LED to indicate charging status (off/charging/complete). It comes pretrimmed for a Li+ battery-regulation voltage of 4.2V, and a single external resistor can set the output as low as 4.0V.

The MAX1679 comes in an ultra-small 8-pin µMAX package. An evaluation kit (MAX1679EVKIT) is available to speed designs. Prices start at $1.65 (1000-up, FOB USA).

## RS-232 transceiver with ±15kV ESD protection draws 1µA

The MAX221E/MAX221 are single, low-power RS-232 transceivers in small TSSOP packages. Requiring less space and operating power than that of traditional dual transceivers, they are ideal for serial-port diagnostic and maintenance applications requiring only one transmitter and one receiver.

The parts operate from a single +5V supply and draw only 1µA of supply current. When the serial port is idle, Maxim's revolutionary AutoShutdown™ circuitry minimizes the supply current without need for changes in the BIOS or operating system. During active communications, both devices guarantee data rates to 250kbps.

The MAX221E provides ESD protection for all RS-232 I/O pins: to ±15kV per the IEC 1000-4-2 Air-Gap Discharge method, to ±8kV per the IEC 1000-4-2 Contact Discharge method, and to ±15kV per the Human Body Model.

The MAX221/MAX221E are available in 16-pin TSSOP and SSOP packages, with prices starting from $1.10 (1000-up, FOB USA).

*AutoShutdown is a trademark of Maxim Integrated Products.*

## 3.0V, 1µA RS-232 transceivers have ±15kV ESD protection

The MAX3386E/MAX3387E RS-232 transceivers have a $V_L$ pin that allows them to operate with various logic levels. Pin-programming the input- and output-logic levels via the $V_L$ pin eliminates the need for level shifters in mixed-logic systems. All RS-232 inputs and outputs are protected to ±15kV using the IEC 1000-4-2 Air Gap Discharge method, to ±8kV using the IEC 1000-4-2 Contact Discharge method, and to ±15kV using the Human Body Model.

A proprietary low-dropout transmitter output stage and dual charge pump enables true RS-232 performance over the full +3.0V to +5.5V supply, and the devices draw only 1µA supply current in shutdown mode. Each device guarantees a 250kbps data rate, and the charge pump requires only four small 0.1µF capacitors. The MAX3386E has two receivers and three transmitters, and the MAX3387E has three of each.

The MAX3386E/MAX3387E are available in space-saving 20-pin TSSOP packages, with prices starting at $2.52 (1000-up, FOB USA).

# NEW PRODUCTS

## Single-supply linear PAs reduce CDMA current draw 50%

The MAX2264–MAX2269 single-supply power amplifiers (PAs) operate from +2.7V to +5.0V supplies. They are designed for PDC, IS-98-based CDMA, and IS-136-based TDMA cellular phones operating in the 900MHz range. The PAs are optimized for highest efficiency at low and medium output power—an important feature for CDMA phones, which deliver less than +16dBm during 90% of their operating time.

When matched for CDMA operation and biased with margin over the adjacent and alternate channel specifications (-45dBc/-56dBc), the MAX2265 achieves up to 29.5dBm output power with 37% efficiency. Its 7% efficiency at +16dBm outputs still yields an excellent overall talk time. The MAX2264's efficiency at that power level is an unprecedented 12%, beating even the most sophisticated dynamic biasing schemes. After adding one external low-cost switch, the MAX2266/MAX2269's efficiency at +16dBm is an even higher 17%. At maximum output power, the MAX2264's efficiency is 32%.

These PAs have internally referenced bias ports, normally terminated with simple resistors, which allow customization of the ACPR margin and gain. These ports can also be used to "throttle back" the bias current when generating low power levels. These devices require no drain switch and no externally applied positive or negative bias voltages. For ease of use, their logic inputs—shutdown pin included—can be driven directly from CMOS logic.

Excellent gain stability over temperature for these devices (±0.8dB) further increases the phone's talk time by dramatically reducing the excess driver current and minimizing overdesign of the driver stages. Nonlinear efficiency when matched for linear operation is 48%. When matched for nonlinear operation only, the nonlinear efficiency is 55%.

The MAX2264–MAX2269 come in 16-pin TSSOP packages with exposed paddle. The MAX2264 is also available in die form for module or direct chip attach (DCA) applications. Prices start at $3.56 (1000-up, FOB USA).

## CDMA IF demodulators integrate VCOs and synthesizer

The MAX2310/MAX2312/MAX2314/MAX2316 IF receivers are designed for dual-band, dual-mode, and single-mode N-CDMA and W-CDMA cellular phone systems. A key feature of this series is its high level of integration. The receivers guarantee +2.7V operation and include a signal path consisting of a variable-gain amplifier (VGA) and I/Q demodulator. The devices have high input IP3 (-33dBm at 35dB gain, 1.7dBm at -35dB), and over 110dB of gain-control range.

Unlike comparable devices, the MAX2310 receiver includes dual oscillators and synthesizers that form a self-contained IF subsystem. To enable dual-band system architectures using any common reference and IF frequency, the synthesizer's reference and RF dividers are fully programmable via a 3-wire serial bus. The differential baseband outputs have sufficient bandwidth for both N-CDMA and W-CDMA systems, and they offer 2.7Vp-p saturated output levels at a low supply voltage of +2.75V.

The MAX2310/MAX2312/MAX2314/MAX2316 come in 28-pin QSOP packages. Prices start at $4.02 (1000-up, FOB USA).

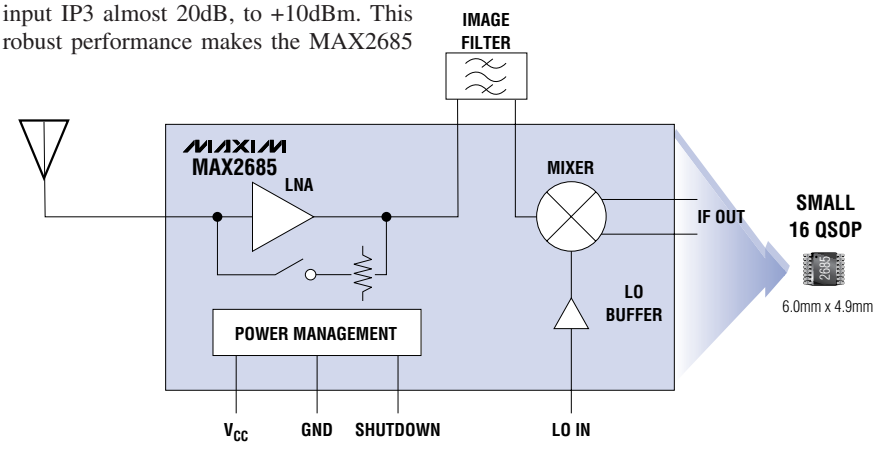
## 900MHz LNA/mixer has best linearity available at 8mA

The MAX2685 is an LNA/mixer IC optimized for best linearity (or input IP3) for 8mA at 900MHz. Its high input IP3 improves a receiver's ability to detect wanted signals under high-interference conditions. This capability is especially important in today's crowded 900MHz spectrum.

The MAX2685 features a combined front-end performance of 21.1dB gain, 2.97dB noise figure, and -9.5dBm input IP3. (This input IP3 is 1dB to 9dB higher than that of GaAs and silicon competitors, resulting in a four-times (6dB) improvement in receiver dynamic range.) A logic-controlled LNA-bypass switch can reduce the LNA gain by 27dB, which increases the input IP3 almost 20dB, to +10dBm. This robust performance makes the MAX2685 ideal for applications such as AMPS, TDMA, and GSM cellular phones, digital cordless phones, private mobile radios, and 868MHz/900MHz ISM-band radios.

The MAX2685 also features an internal LO buffer that allows the LO port to be driven with a low (-8dBm) LO signal. The low operating-supply range (2.7V to 5.5V) and a low supply current of 8.5mA (high-gain mode) or 3.8mA (low-gain mode) make the device suitable for use in applications powered by 3-cell NiCd or 1-cell Li+ batteries. A low-power shutdown mode further extends battery life by reducing the supply current below 0.1µA.

A fully assembled evaluation kit (MAX2685EVKIT) is available to help reduce design time. The MAX2685 comes in a space-saving 16-pin QSOP package, with prices starting at $1.37 (1000-up, FOB USA).



# NEW PRODUCTS

## Dual-band SiGe LNA/mixer ICs offer low noise and high linearity

A new family of SiGe ICs for receiver front-ends (MAX2320/MAX2324/MAX2326/MAX2327/MAX2329) sets an industry standard for noise, linearity, and supply current in the LNA/mixer function in CDMA, W-CDMA, TDMA, PDC, and GSM cellular phones. New and unique features incorporated in this MAX2320 family include integrated VCO doublers or dividers, VCO buffers, dual LNA gain settings, independently adjustable LNA and mixer linearity, and a pin-selectable, low-current paging mode that extends phone-standby time. All devices operate with a single +2.7V to +3.6V supply.

Four devices operate at both cellular and PCS frequencies, one at cellular only, one at PCS only, and one is configured as a dual PCS device. Each includes an LNA with high input IP3, which minimizes cross-modulation in the presence of large interfering signals. The ICs provide both a low-gain mode that bypasses the LNA to provide higher cascaded IIP3 at low current, and a high-gain, low-current mode that extends the phone-standby time for pagers.

All devices are available in 20-pin TSSOP-EP packages (exposed paddle). Prices start at $2.77 (1000-up, FOB USA).

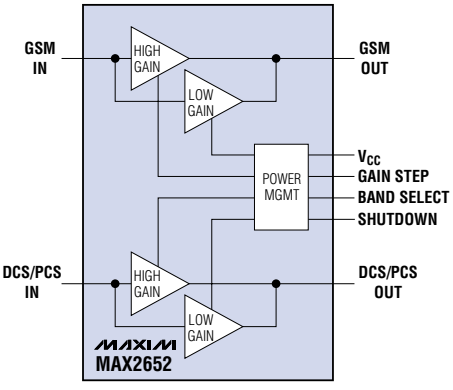
## SiGe dual LNA increases sensitivity for GSM dual-band phones

The MAX2651/MAX2652/MAX2653 SiGe low-noise amplifiers (LNAs) are capable of operation at the GSM900, DCS1800, and PCS1900 bands. Fabricated with Maxim's advanced SiGe bipolar process, these LNAs provide a very low noise figure, high gain, and high linearity. To further improve the receiver sensitivity and dynamic range in today's GSM dual-band and triple-band cellular phones, they include a 20dB attenuation step.

The MAX2651/MAX2652 consist of two LNAs. One LNA is optimized for the GSM900 band, providing a high gain of 18dB and a low noise figure of 1.2dB. The other is optimized for the DCS1800 band, providing a low 1.8dB noise figure and a high gain of 18dB. The MAX2652 offers an additional low-power shutdown mode. Its packaging is the smallest in the industry for this type of product: the 10-pin µMAX measures only 4.9mm x 3.0mm including leads.

The MAX2653 consists of one LNA optimized for operation at both the DCS1800 and PCS1900 bands. It provides a 1.7dB noise figure and 18.5dB gain at the DCS band, or 1.8dB noise figure and 18.5dB gain at the PCS band. It also comes in an 8-pin µMAX package with the same footprint as the 10-pin µMAX. In addition, the MAX2653 features a 1µA low-power shutdown mode.

All devices operate on a single +2.7V to +3.3V supply . They draw 6mA to 8mA in the high-gain mode and 2.2mA in the low-gain mode. Prices start $1.19 (1000-up, FOB USA). Fully assembled evaluation kits are available to help reduce design time.




## 4-channel interconnect simplifies rack-to-rack interface

The MAX3831 combines a 4:1 multiplexer with a 1:4 demultiplexer, allowing 2.5Gbps data transmission over a pair of wires or fibers connecting telecommunications equipment. The 3.3V, 2.5Gbps, SDH/SONET device includes a clock generator. It saves space, power, and money by enabling high-speed rack-to-rack, shelf-to-shelf, and card-to-card interconnections with a single pair of fibers. Applications include SDH/SONET backplanes, dense digital cross-connects, and intrarack/subrack interconnects.

Combined with the MAX3876 (a +2.5Gbps clock and data-recovery IC), the MAX3831 forms an ideal high-speed interconnect. The MAX3831 consumes only 1.45W when operating from a single 3.3V supply. It exhibits only $2.5ps_{RMS}$ of random jitter and 8psp-p of deterministic jitter.

The MAX3831 has a 622Mbps SDH/SONET LVDS parallel interface, whose 2.488Gbps serial-CML data streams interface to an optical or electrical driver. Its 10-bit-wide elastic buffer accommodates as much as ±7.5ns of skew between the 155.52MHz external reference clock and any parallel data input. An internal frame detector with TTL loss-of-frame monitor looks for a 622Mbps SDH/SONET framing pattern, and rolls the demultiplexer to maintain proper channel assignments at the outputs. The MAX3831 provides a 622MHz LVDS clock output.

High-speed built-in self-testing (BIST) is provided by an on-chip pattern generator, and flexibility in system test is provided by system- and line-loopback modes. The MAX3831 comes in a 64-pin TQFP exposed-paddle package, with prices starting at $29.95 (1000-up, factory direct, USA). Evaluation kits are available (specify MAX2651EVKIT, MAX2652-EVKIT, or MAX2653EVKIT).

# NEW PRODUCTS

## Clock and data-recovery IC exceeds SDH/SONET specifications

The MAX3676 is a 622Mbps, 3.3V clock-recovery and data-retiming IC with limiting amplifier. Designed for both section-regenerator and terminal-receiver applications in SDH/SONET OC-48/STM-16 transmission systems, it surpasses all ITU/Bellcore jitter specifications. When combined with the MAX3665 transimpedance amplifier and the MAX3681 1:4 deserializer, it forms a complete, high-performance 622Mbps receiver.

The MAX3676 operates from a single supply in the +3.3V to +5.0V range, and consumes only 237mW at 3.3V. Its jitter generation is less than the SDH/SONET specification by 8.0mUI$_{RMS}$. Jitter tolerance at 1MHz exceeds the SDH/SONET specification by 0.54UIp-p.

The MAX3675 offers selectable data inputs: one input accepts PECL levels, and the other accepts small-signal analog levels. Analog inputs access the limiting amplifier stage, which provides both a received-signal-strength indicator (RSSI) and a programmable-threshold loss-of-power (LOP) monitor. Selecting the PECL amplifier conserves power by disabling the limiting amplifier.

The fully integrated phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input, which in turn is retimed by the recovered clock. Both clock and data signals have differential PECL outputs. The fully integrated PLL also incorporates a loss-of-lock (LOL) monitor.

An evaluation kit (MAX3676EVKIT) is available to shorten design time. The MAX3676 comes in a 32-pin TQFP package, with prices starting at $15.00 (1000-up, factory direct, USA).

## Low-power, 3V, 2.5Gbps serializer includes clock synthesis

The MAX3890 is a 16:1 serializer with clock synthesis and LVDS inputs. A 3.3V SDH/SONET device operating at 2.5Gbps, the MAX3890 is ideal for converting 16-bit-wide, 155Mbps parallel data to 2.5Gbps serial data in SDH/SONET and ATM applications. Combining the MAX3890 with the MAX3867 laser driver (which includes APC), the MAX3866 TIA and limiting amplifier, and the MAX3880 1:16 deserializer with clock recovery, forms a complete, four-chip, 2.5Gbps transceiver.

The MAX3890 has the lowest power consumption (495mW) of any available 2.5Gbps serializer with clock generator. The maximum generated jitter (3ps$_{RMS}$) provides a margin of 1ps$_{RMS}$ with respect to the ITU/Bellcore SDH/SONET specification. Operating from a single +3.3V supply, the MAX3890 accepts low-voltage differential-signal (LVDS) clock and data inputs for interfacing with high-speed digital circuitry, and delivers PECL serial data and clock outputs.

An internal, fully integrated PLL synthesizes a 2.5GHz serial clock from a reference clock of 155.52MHz, 77.76MHz, 51.84MHz, or 38.88MHz. A loopback data output simplifies system diagnostic testing. The MAX3890 comes in a 64-pin TQFP exposed-paddle package, with prices starting at $69.90 (1000-up, factory direct, USA). Evaluation kits are available (MAX3890EVKIT).

## First triple-voltage supervisors in SOT23 packages

The MAX6355/MAX6356 are the first microprocessor supervisory circuits in a 6-pin SOT23 package capable of monitoring up to three voltages. By reducing external components and adjustments, they reduce board space and cost while increasing reliability.

The MAX6355 and MAX6356 monitor two factory-set voltages (either 5V and 3.3V or 3.3V and 2.5V), and a third voltage that can be set by the customer with an external resistor-divider. They also include a debounced manual-reset input.

MAX6355/MAX6356 devices draw only 20µA of supply current, and their reset-threshold accuracy over temperature is 2.5%. When any of the three monitored voltages declines below its threshold, the device asserts a reset signal and maintains it for a minimum of 100ms after $V_{CC}$ returns above the threshold (or until the manual reset is deasserted). The MAX6355 has an open-drain, active-low $\overline{\text{RESET}}$ output, and the MAX6356 has a push-pull, active-low $\overline{\text{RESET}}$ output. Both reset outputs are guaranteed valid to 1.0V.

The MAX6355/MAX6356 are each available in two standard versions. They come in 6-pin SOT23 packages and in 2500-piece order increments. For availability of nonstandard versions, which come in 10,000-piece order increments, please contact the factory. Prices start from $1.38 (2500-up, standard versions only, FOB USA).